

## Digital Video Interfacing Products

# AT400PCI

DVB-ASI input and output  
DVB-SPI Input and output



## Standard Features

- **PCI 2.2**, 32 bit, 33/66MHz 3.3V.
- Bus Master DMA, Scatter /Gather Interface Protocol.
- Windows 2000, XP and **Linux** Drivers.
- Accompanied by DVSStaion2, Alitronika's Integrated TS Player, Recorder & Real Time Quick Analyser Software.
- Supports DVB Standards **A1010Rev1** and **EN50083**.
- Supports 188 /204 byte Packet Sizes.

### Input

- Integrated Loop Through output.
- Supports True or Inverted ASI signals.
- Carrier and Lock Detection.
- Sync, Error & Code Violation Detection.
- Automatic Cable Equalization of up to 350m.
- Support for Time Stamping, PID filtering.

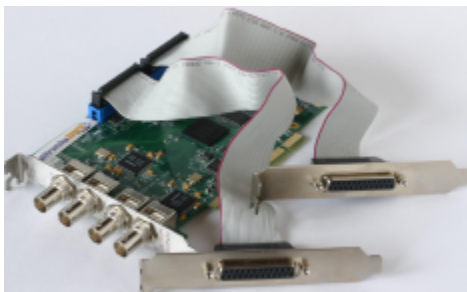
### Output

- **Two** DVB-ASI and **One** DVB-SPI outputs.
- Programmable Output Bit Rate.
- Null Packet Insertion by hardware.
- Selectable Burst size mode & continuous mode TS output.
- Hardware TS generation.

## Application

*Targeted for Digital Video Professionals, Sophisticated End Users and OEMs the AT400PCI is an ideal solution for A number of applications such as:*

- Development Tools.
- DVB to IP or IP to DVB Gateway.
- Transport Stream Recording.
- Transport Stream Playing.
- Transport Stream Analysing
- Transport Stream Monitoring.
- Video on Demand Server.
- Transport Stream Test Generator.
- High Speed Serial Data Link.
- Serial (ASI) to Parallel (SPI) and Parallel to Serial Conversion.
- One (ASI) to 3 ASI & 1 SPI signal multiplier.



## Specifications

**On Board Buffer:** 16Mbytes  
**Serial Connectors:** 75 Ohms BNC  
**Input Return Loss:** >15 dB  
**Input Signal level:** 800 mV +/- 10%  
**Output Signal level:** 1.0Vp-p nominal  
**Parallel Connectors:** 25-pin sub-D  
**DVB-ASI Input/Output Bit Rate:** 0 to 214 Mbit/s  
**DVB-SPI Input/Output Bit Rate:** 0 to 108 Mbit/s  
**Bit Rate Stability:** +/- 25ppm  
**DVB-ASI Input/Output Clock:** 270 MHz  
**DVB-SPI Input/Output Clock:** 0 to 13.5 MHz  
**DVB-SPI Input/Output Level:** LVDS  
**Size WxL:** 175mmx107

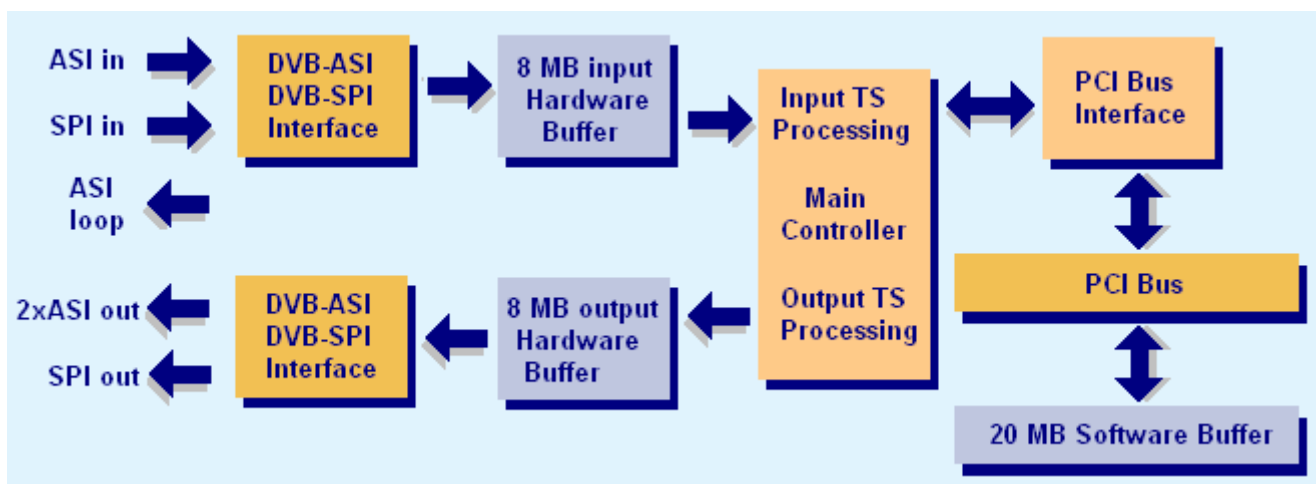
## 1 GENERAL DESCRIPTION

*A member of Alitronika's state of art digital video interfacing products.*

The AT400PCI is a PCI based interface device suitable for Recording, Playing and Analyzing of DVB-ASI Transport Streams.

## 2 BLOCK DIAGRAM

**FIG4** illustrates the block diagram of the AT400PCI device. The device communicates with the PC via the UPCI interface device. On the input side, the serial data is de-serialized 8b/10b and de-coded before it is presented to PC via the PCI controller device. On the output side, the MPEG-II transport streams enter the device via the PCI interface device. The AT400PCI then transmits the transport streams according to the settings provided by the application software. The data is 8b/10b encoded for DVB-ASI signals before it is serialized and transmitted via the BNC output connectors.



## 3 EXTERNAL INTERFACES

The external interfaces for the AT400PCI are shown. There are 4 BNC connectors for the Serial, DVB-ASI, input and outputs and 2 box headers (seen in blue in the picture) for DVB-SPI input & output. The Unit is supplied with two flat cable/D-type/ bracket combination for access to the DVB-SPI ports.



The LED in the back of the unit function as follows:

**OFF** = Power is off/ device not activated

**Flashing (Red)** = Play /Record not activated – Error condition

**ON (Green)** = Normal operational condition

In Record mode this LED indicates that a Carrier has been detected and the device has locked to incoming TS.

In Play mode this LED indicates that the output section has valid TS (normal operating conditions).

## 4 APPLICATION

Targeted for digital video professionals, sophisticated end users and OEMs the AT400PCI is an ideal solution for a number of applications such as, development tools, universal interface for MPEG-II Transport Stream Playing and Recording, video on demand server, transport stream test generator, high speed serial data link, software based MPEGII decoders & encoders and many other applications.

## 5 HARDWARE DESCRIPTION

### 5.1 PCI interface device & PCI standards

The PLX Technology device, PCI-9056, is used as the PCI interface. PCI-9056 is a, PCI r2.2 compliant, bus mastering interface between PCI bus and 32-bit, 66 MHz processor Local Bus. This device implements the bus master DMA, scatter/ gather interface protocol. Please refer to PCI 9056B Data book, Version 1.1 for more information about the operation and register setting of this device. Alitronika Digital Interfacing Products comply with PCI r2.2 standard as defined by these specifications for more information please refer to PCI r2.2 document.

### 5.2 Main Controller

For the main controller the Altera Cyclone FPGA device is used. Most of the function of the AT400PCI is carried out by the firmware residing in this device. The main controller configures and communicates with the various devices on board the AT400PCI device. It carries out all the transport stream processing required by the application software, including data buffering, clock synthesizer, synchronization to the transport stream, time stamping, error flag generation, bit rate estimation and others.

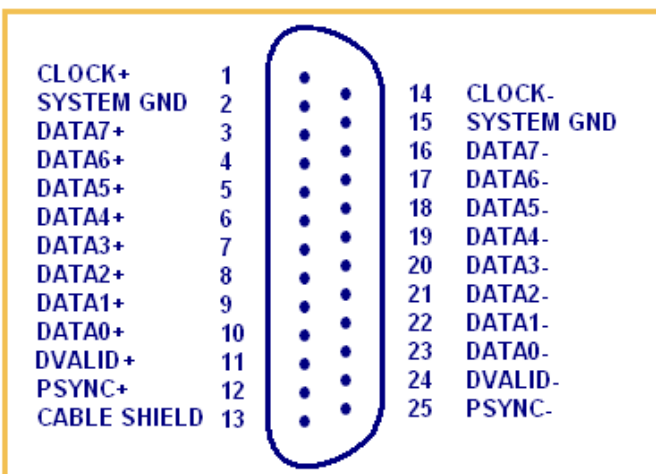
### 5.3 Configuration Scheme

The FPGA on board most devices use SRAM configuration elements that require configuration data, better known as the firmware, to be loaded each time the device powers up. This process is called configuration. The description of configuration schemes used for such devices is beyond the scope of this document. A configuration device is almost always used. The devices are configured whenever the PC is powered up. Often this process is not carried out successfully and the device is not fully operational, the system must then be reset. Alitronika interface devices have provision for such a scheme, so it could be implemented on all the products if requested. But a much better scheme, whereby the configuration data is loaded by the application via the device driver is used. This gives Alitronika's products the flexibility that the firmware could be up-graded, customized and up-dated. More importantly, more than one firmware could be and has been developed for each device.

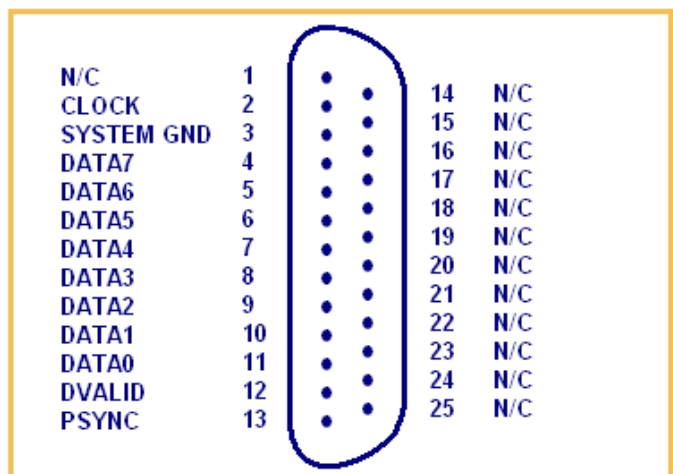
Instead of the FPGA being configured on power up, it could be configured at all times by the application, without the need for resetting the system. This method is called dynamic configuration scheme and places Alitronika's products at the top when it comes to flexibility and reliability.

#### Parallel ( DVB-SPI) Pinouts

For Alitronika's devices which support DVB-ASI input/output ( LVDS and/or LVTTTL/LVCMOS )



Standard DVB-SPI input/output Pinout



LVTTTL/LVCMOS output Pinout

### 6.1 The Serial Input (DVB-ASI)

The serial input section consists of mainly buffers, filters and the Cable equalizer device.

#### 6.1.1 The Cable equalizer

The Gennum GS9064 Adaptive cable equalizer device is used to equalize and restore the input signal over 75Ohm co-axial cable optimized for performance at 270Mb/s. The cable equalizer section is designed to provide automatic cable equalization for cable length of up to 300 meters.

### 6.2 Loop through serial output

A serial loop through output with integrated cable driver is provided for looping through the serial input during recording. The cable driver features an output mute on loss of signal, high impedance mode and adjustable signal swing. The output BNC connector is used for the loop through output during recording.

### 6.3 The parallel input (DVB-SPI)

The DVB-SPI input is to a LVDS levels according to DVB-SPI standards.

### 6.4 Input Transport stream processing

The Input data processing module, implemented in firmware, resides inside the main controller and carries out most of the input data processing. These include the following:

#### 6.4.1 Packet size detection

The AT400PCI can accept both 188 and 204 bytes packets. The 188 or 204 packet size flag is then set high accordingly.

#### 6.4.2 Data Error Indication

Every byte of the transport packet which can not be decoded due to errors are indicated to the input transport stream processing unit. These errors are counted by a free running Data Error Counter and are presented to the application and are then displayed during recording and monitor modes. In addition a data error flag is raised when the number of errors are more than the number of acceptable errors for the integrity of the serial link to be maintained.

#### 6.4.3 Sync Loss Error

The Packet Synchronizer Algorithm within the input transport stream processor, monitors the synchronization byte of the transport stream, H"47", if it does not find it at the start of a packet, it indicates it to the application software in record and monitor modes by means of a Sync Loss Counter.

#### 6.4.4 Input Transport Stream Bit Rate Estimation.

The input transport stream bit rate is obtained from the PCR. In cases such as RAW data mode the bit rate is estimated by counting the number of received packets in a certain time period and the calculating the bit rate.

#### 6.4.5 Time Stamping

There are applications in which it is important to know the time of arrival of the transport packets. These applications include, real-time transport stream processing e.g. PCR correction, BRT (Bit Rate Trans-coding) and re-multiplexing of transport streams. The time of arrival of a transport packet is when the PCR byte, the 11<sup>th</sup> byte of the transport stream, enters the input data processing module.

The time stamp is derived from a 32bit reference clock counter running at the master clock frequency of the main controller.

On arrival of the 11<sup>th</sup> byte of the transport stream, the content of this counter is taken.

This 32bit time stamp value is then added to the end of the transport packet, hence creating a transport packet of 192 for a 188 byte packet or 208 byte for a 204 byte packet size.

#### 6.4.6 PID Filtering

The AT400PCI supports PID filtering. In order to avoid having long PID tables, two modes of PID filtering are used, Exclusive & Inclusive. In exclusive mode PIDs in the table are filtered out and in inclusive mode the PIDs in the table are kept and all other PIDs are removed.

#### 6.4.7 RAW data mode

AT400PCI can receive none DVB TS files of any kind to be played back. In this mode the AT400PCI acts as fast serial data interface.

#### 6.4.8 Data Buffering

It is beyond the scope of this document to explain the trivial details of streaming and buffering of the MPEG-II transport streams. It is sufficient to state that a DMA buffer is used to transfer data to the PC from the AT400PCI device rather than direct read cycles. In addition to this software buffer, the AT400PCI uses an 8Mbytes of SDRAM to implement a hardware input FIFO buffer. Two or three other internal FIFO's are used by the main controller for smooth recording of the transport streams. In addition there are two 10Mb software buffers. The application software indicates the buffer usage during recording.

## 7 OUTPUT

### 7.1 The Serial Output (DVB-ASI)

The serial output section consists of mainly buffers, filters and a line driver device.

### 7.2 The Parallel Output (DVB-SPI)

The Parallel output section consists of LVDS according to DVB-SPI standards.

### 7.3 Transmit FIFO Buffer

An 8Mbytes SDRAM is used to implement the transmit buffer. The buffer enables the AT400USB to generate low jitter DVB-ASI stream by compensating for any Bus latencies.

In addition to this rather large FIFO, two or three other internal FIFO's are used by the main controller for smooth transmission of the transport streams. There are also two 10Mb software buffers. The application software indicates the buffer usage during playing.

### 7.4 On board transmission clock and clock Synthesizer

An accurate 27MHz clock generator on board the AT400PCI is used for the transmission of the output stream.

The byte rate clock of the transmitted transport stream is obtained from this clock using a clock synthesizer. Unlike other so-called "direct-digital synthesizers", the clock synthesizer on board AT400PCI is not made up of a simple accumulator. It is based on a sophisticated algorithm to generate an accurate, jitter free output transmission even at high bit rates. The clock synthesizer obtains the transmission bit rate set by the application software, and generates a transmit pulse, which could be regarded as the byte rate for DVB-ASI transmission. One byte of the payload per transmit pulse is transmitted. In between these transmit pulses the controller transmits the stuffing character, K28.5 (Comma). For the DVB-SPI, the synthesizer generates a byte rate clock from the numerical bit rate value. Here as the DVB-SPI standards require a 10 bit data is transmitted per clock with no stuffing allowed.

### 7.5 Transport packet size

AT400PCI can transmit packet sizes of 188 or 204 bytes, in addition if desired it can generate a 204 byte transport packet from a 188 byte packet by adding 16 zero bytes to the end of the payload. This function is useful for the designers of receiver equipments to test if the system under development could handle both 188 and 204 packet sizes. The application software corrects the PCR accordingly.

### 7.6 Burst mode and Continuous mode

AT400PCI can transmit transport stream in continuous mode in which the bytes are spread with stuffing "Comma" character filling the stream when there are no payloads. In the burst mode the transport packets are transmitted in user selectable burst sizes of up to the full packet size (188 or 204).

### 7.7 Null packet insertion by hardware

AT400PCI allows the transmitted bit rate higher than of the bit rate of the transport stream file. In such cases the difference between the default bitrate and play bitrate is filled with Null packets. The application software corrects the PCR accordingly.

### 7.9 RAW data mode

AT400PCI can play back none DVB TS files of any kind to be played back. In this mode the device acts as fast serial data interface.

### 7.10 Serial to Parallel & Parallel to Serial conversion.

The AT400PCI having both DVB-ASI and DVB-SPI inputs and output is cable of converting from DVB-SPI to DVB-ASI or vies versa.

### 7.11 Signal multiplier (simple router)

Since the AT400PCI has two serial and one parallel outputs as well as a loop through output, an input signal could be looped through and pass through hence creating a 1 to 3 signal multiplier. At the same time if the ASI to SPI conversion is enabled, the parallel output could also be used

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